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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/708,943	04/02/2004	Long-Hui Lin	LKSP0028USA	2942

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EXAMINER	
GUTIERREZ, ANTHONY	

ART UNIT	PAPER NUMBER
2857	

NOTIFICATION DATE	DELIVERY MODE
02/26/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/708,943	LIN, LONG-HUI	
	Examiner	Art Unit	
	ANTHONY GUTIERREZ	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 November 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Art Unit: 2857

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 2, and 6-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Nozoe et al. (United States Patent: US 6,777,677 B2).

As to claim 1, Nozoe et al. discloses a method of defect root cause analysis (col. 4, lines 12-34) comprising: providing a die being processed through a plurality of semiconductor processes (see Fig 6, 7A, and 7B which includes a plurality of dies on a single wafer that undergo the foregoing processes), wherein the die comprises a plurality of defects (see the dots on the Figures mentioned above and col. 4, lines 35-47); dividing the defects into three defect types (col. 10, lines 51-60) comprising a first defect type (figure defect), a second defect type (flaw), and a third defect type (disconnection/short circuit) according to their sizes and locations (col. 9, lines 55-63); performing a defect inspection to detect sizes and locations of the plurality of defects (col. 4, lines 59-62); using three methods to perform a chemical state analysis corresponding to each defect type respectively (Figs 5 and 6 and related discussion beginning at col. 16, line 6, in which the first method (Figure Review Mode) performs the chemical state analysis (using a beam current of 3pA-50pA, and a beam irradiation energy of 800v-1kV) corresponding to the figure defect type, the third method (Voltage Contrast Review Mode) performs the chemical state analysis (using a beam current of 50pA-200pA, and a beam irradiation energy of 500v-800V) corresponding to the disconnection/ short circuit defect type, and the second method (Roughness Review Mode) performs the chemical state analysis for the flaw defect type; see also col. 15, lines 24-47); performing a mapping analysis according to a result of the chemical state analysis, wherein the mapping

analysis comprises: forming the defects of the die into a defect pattern; and comparing the defect pattern with a predetermined pattern on the die; and analyzing the root cause of the defects according to the comparison between the defect pattern and the predetermined pattern on the die for determining the semiconductor process causing the defect(col. 10, lines 5-33, and col. 12, lines 31-51); and modifying the semiconductor process causing the defects to reduce the number of detects in the die (col. 19, lines 45-50 and col. 20, lines 46-50).

As to claim 2, in addition to the features rejected above with respect to claim 1, Nozoe et al. discloses comprising performing a defect classification after finishing the defect inspection for judging a defect type of the defects and performing a corresponding chemical state analysis according to the defect type of the defects (col. 10, lines 19-33).

As to claim 6, in addition to the features rejected above with respect to claim 1, Nozoe et al. discloses that the chemical state analysis comprises (see col. 9, line 66-col. 10, line11) a point scan analysis (SEM), delayer analysis (AES), and depth profile analysis (TEM).

As to claim 7, Nozoe et al. discloses a method of defect root cause analysis (col. 4, lines 12-34) comprising following steps: providing a die being processed through a plurality of semiconductor processes (see Fig 6, 7A, and 7B which includes a plurality of dies on a single wafer that undergo the foregoing processes), wherein the die comprises a plurality of defects (see the dots on the Figures mentioned above and col. 4, lines 35-47); performing a voltage contrast to identify locations of the defects (col. 4, lines 59-62); cutting the die with a focus ion beam (FIB) to expose a cross-section of the die (col. 9, line 67-col. 10, line 2); utilizing auger electrons to perform a chemical state analysis of the cross-section of the die (col. 10, lines 3 and 4); performing a mapping analysis according to a result of the chemical state analysis wherein the mapping analysis (col. 10, lines 5-33, and col. 12, lines 31-51) comprises: forming the defects into a defect pattern (col. 18, lines 40-51 and Figs. 7A and 7B with respect to the review sequence) and comparing the defect pattern with a predetermined pattern on the die; judging a root cause of the defect generation according to the comparison between the defect pattern and the predetermined pattern on the die for determining the semiconductor process causing the defect (col. 10, lines 51-60, col. 13, lines 45-55, col. 15, lines 34-41 and col. 3, lines 9-15) and modifying the

semiconductor process causing the defects to reduce the number of detects in the die (col. 19, lines 45-50 and col. 20, lines 46-50).

As to claim 8, in addition to the features rejected above with respect to claim 7, Nozoe et al. further discloses that the method utilizes an auger electron spectroscopy (AES) to perform a chemical state analysis of the cross-section of the wafer (col. 10, line 4).

As to claim 9, in addition to the features rejected above with respect to claim 7, Nozoe et al. further discloses the chemical state analysis comprises a point scan analysis (SEM of col. 9, line 66-col. 10, line 5).

As to claim 10, in addition to the features rejected above with respect to claim 1, Nozoe et al. discloses wherein the first defect type comprises defects located on an underlayer of the die (col. 9 lines 30-34).

As to claim 11, in addition to the features rejected above with respect to claim 1, Nozoe et al. discloses wherein the second defect type comprises defects located on the surface of the die and are thick particles (col. 15, lines 45-48).

As to claim 12, in addition to the features rejected above with respect to claim 1, Nozoe et al. discloses wherein the third defect type comprises defects located on the surface of the die and are not thick particles. (col. 15, lines 34-45).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nozoe et al. (United States Patent: US 6,777,677 B2), in view of Moore et al. (United States Patent: US 6,777,674 B2).

As to claim 3, in addition to the features rejected above with respect to claim 1, Nozoe et al. discloses the use of auger analysis for detecting defects in a semiconductor wafer (col. 10, line 4 of Nozoe et al.).

Nozoe et al. does not specifically disclose that the auger analysis is performed when the defects are not single phase particles.

Moore et al. however discloses that Auger analysis can be employed to provide phase information on chemical bonding of elements. This implies that the particles are not single-phase particles, since the analysis is needed to determine the phase information. Moore et al. further teaches that this analysis is advantageous for small diameter particles with respect to surface sample analysis (col. 2, lines 46-59).

It therefore would have been obvious to one of ordinary skill in the art at the time of invention to use Auger analysis, as disclosed by Nozoe et al., for non-single phase defects, as taught by Moore et al., to advantageously determine chemical bonding information related to small particle defects on the surface of the wafer, in order to more accurately determine the effect that a small particle has on the relationship of the bonding of wafer surface elements, thereby facilitating removal of the particle without damaging the wafer.

As to claim 4, in addition to the features rejected above with respect to claim 3, Nozoe et al. specifically discloses that the auger analysis is auger electron spectroscopy (AES) for detecting defects in a semiconductor wafer (col. 10, line).

As to claim 5, in addition to the features rejected above with respect to claim 1, Nozoe et al. discloses the use of auger analysis for detecting defects in a semiconductor wafer (col. 10, line 4).

Nozoe et al. does not specifically disclose that an energy dispersive spectrometer (EDS) is utilized when the defects are thick particles.

Moore et al. however discloses an interchangeability between Auger and EDS techniques (col. 3, lines 23-43), and further teaches that EDS is beneficial for application with respect to relatively heavier particles than those for which Auger analysis would be beneficially (col. 2, lines 65-67).

It therefore would have been obvious to one of ordinary skill in the art at the time of invention to employ EDS techniques in place of Auger techniques, for thick particles, in order to facilitate the removal of a heavier particle, without risking background contamination that are common in Auger techniques, as taught by Moore et al. (col. 3, lines 1-16).

Response to Arguments

5. Applicant's arguments with respect to claims 1-12 have been considered but are moot in view of the new ground(s) of rejection.

While Applicant's amendment has overcome the rejection under 35 U.S.C. 112, first paragraph, the Examiner maintains that the prior art of record provides anticipation or renders obvious Applicant's claimed invention as addressed above with respect to the recent amendment.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to ANTHONY GUTIERREZ whose telephone number is (571)272-2215. The examiner can normally be reached on Monday to Thursday, 8:30 AM-7:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eliseo Ramos-Feliciano can be reached on (571) 272-7925. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/AG/

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2/14/08

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